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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,554	08/30/2001	Leonard Forbes	1303.028US1	1837

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EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 12/13/2002

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/945,554

Applicant(s)

FORBES, LEONARD

Examiner

Thomas L Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) 13-18 and 28 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-27, 29-32 and 39-42 is/are allowed.
- 6) ☐ Claim(s) 1-6, 9, 10, 33-36, 43, 44, 47 and 48 is/are rejected.
- 7) ☒ Claim(s) 7, 8, 11, 12, 37, 38, 45, 46 and 49 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. The preliminary amendment filed on 01-16-02 has been entered.

Election/Restriction

2. Applicant's election without traverse of Embodiment 1, claims 1-12, 19-27, and 29-49 reading thereon, in paper # 7, is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 12/31/01 is acceptable.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the one or more SRAM cells, each cell comprising at least a pair of cross coupled NMOS floating gate transistors; a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors; and a pair of wordlines coupled to the pair of access transistors, as recited in claims 19, 24, 29 and 39, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

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A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

5. Applicants have made no claim for priority.

Information Disclosure Statement

6. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

7. The disclosure is objected to because of the following informalities:

On page 1, an attempt to recite the title of the invention contains a typo; "DRAM" should be –SRAM–. Also on page 1 the serial numbers should be amended as follows:

Attorney Docket Number:	Serial Number:
1303.019US1	09/945395
1303.020US1	09/943134
1303.024US1	09/945498
1303.027US1	09/945512
1303.014US1	09/945507

Also on page 1 there are two references to Attorney Docket Number 1303.019US1. The second reference to Attorney Docket Number 1303.019US1 ap-

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appears to be a reference to "SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS," which is actually Attorney Docket Number 1303.028US1. This title references the instant application and should be removed from the list of related applications.

The disclosure is objected to because of the following informalities: The Detailed Description of the invention does not include a description of the one or more SRAM cells, each cell comprising at least a pair of cross coupled NMOS floating gate transistors; a pair of bitlines coupled to the pair of cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors; and a pair of wordlines coupled to the pair of access transistors, as recited in claims 19,24,29 and 39, nor details of the making of said cells, nor details of how said cells are used.

Appropriate correction is required.

Claim Objections

8. Claim 5 is objected to because of the following informalities:

Claim 5, which recites dependency from claim 3, refers to the antecedent term "transition metal oxide," which does not appear in claim 3 but does appear in claim 4. Claim 5 will be examined as if it recited dependency from claim 4. Claim 5 must be amended to avoid the apparent lack of an antecedent basis for "transition metal oxide."

Appropriate correction is required.

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Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1,2, and 33 are rejected under 35 U.S.C. 102(a) as being anticipated by FORBES et al. (6,141,248).

Forbes et al. discloses a memory cell, or a method for making the same, with a pair of cross coupled inverters 206-308 and 210-312, wherein each inverter includes an NMOS transistor 308,312 and a PMOS transistor 206,210, and wherein at least one of the NMOS transistors 308,312 includes: a first source/drain region 118 and a second source/drain region 122 separated by a channel region 120a in a substrate 120; a floating gate 116 opposing the channel region 120a and separated therefrom by a gate oxide 126; and a control gate 114 opposing the floating gate 116, wherein the control gate 114 is separated from the floating gate 116 by a low tunnel barrier intergate insulator 124; and a pair of bitlines 216,217 coupled to the pair of cross inverters 206-308 and 210-312 at a pair of voltage nodes, wherein the floating gate 116 is adapted to be programmed with a charge such that the memory cell has a definitive asymmetry and a definitive state upon startup, and a conformal method of form-

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ing said memory cell, comprising: forming the said pair of cross coupled inverters 206-308 and 210-312, wherein forming each said inverter includes an NMOS transistor 308,312 and a PMOS transistor 206,210, and wherein the method includes forming at least one of the NMOS transistors 308,312 to include: the said first source/drain region 118 and the said second source/drain region 122 separate by the said channel region 120a in the said substrate 120; the said floating gate 116 opposing the said channel region 120a and separated therefrom by the said gate oxide 126; and the said control gate 114 opposing the said floating gate 116, wherein the said control gate 114 is separated from the said floating gate 116 by the said low tunnel barrier intergate insulator 124 such that the said floating gate 116 is adapted to be programmed with the said charge and the said memory cell can have the said definitive asymmetry and the said definitive state upon startup; and forming the said pair of bitlines 216,217 coupled to the said pair of cross inverters 206-308 and 210-312 at the said pair of voltage nodes. Note figures 5B and 8A and column 5 lines 1-60 of Forbes et al.

B. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by NISHIMURA (6,069,816).

Nishimura discloses a four transistor SRAM cell with floating gate transistors comprising: a pair of cross coupled NMOS floating gate 30 transistors MT1 and MT2, wherein each of the pair of cross coupled NMOS transistors MT1 and MT2 includes: a first source/drain region 22 and a second source/drain region 24 separated by a

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channel region 26 in a substrate 20; a floating gate 30 opposing the channel region 26 and separated therefrom by a gate oxide 28; and a control gate 34 opposing the floating gate 30, wherein the control gate 34 is separated from the floating gate 30 by a low tunnel barrier intergate insulator 32; a pair of bitlines coupled to the pair of cross coupled NMOS floating gate 30 transistors at a pair of voltage nodes through a pair of access transistors ST11 and ST21; and wherein the floating gate 30s are adapted to be programmed with a respective charge state such that the SRAM cell has a definitive asymmetry. Note figures 3A, 3B, and 11 of Nishimura.

C. Claims 43, 44, and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by RATNAKUMAR et al. (5,986,932).

Ratnakumar et al. discloses a method for operating an SRAM cell comprising a method for operating an SRAM cell which includes a pair of cross coupled floating gate transistors P1-N1 AND P2-N2, comprising: writing to at least one of the cross coupled floating gates 226 of the SRAM cell using channel hot electron injection, wherein the cross coupled floating gate transistors each include: a first source/drain region 220 and a second source/drain region 222 separated by a channel region 218 in a substrate; a floating gate 226 opposing the channel region 218 and separated therefrom by a gate oxide 230; and a control gate 224 opposing the floating gate 226, wherein the control gate 224 is separated from the floating gate 226 by a low tunnel barrier intergate insulator 228; erasing charge from the floating gate 226 by tunneling electrons off of the floating gate 226 and onto the control gate 224; and sensing a

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logic state of the SRAM cell in a start up mode. Note figures 4,6 and columns 9 lines 17-29 and 62-67 and column 10 lines 1-27 of Ratnakumar et al.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 3,34,4,35,5, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over FORBES et al. (6,141,248) in view of ADAM (4,295,150).

Forbes et al. discloses a memory cell with floating gate transistors, or a method of making the same, having all the limitations of claims 3,34,4,35,5, and 36 except that the low tunnel barrier intergate insulator includes a metal oxide insulator selected from PbO or Al₂O₃ in claims 3 and 34, a transition metal oxide in claims 4 and 35 or specifically, in claims 5 and 36, a transition metal oxide selected from the group consisting of Ta₂O₅, TiO₂, ZrO₂, and Nb₂O₅. Note figures 5B and 8A and column 5 lines 1-60 of Forbes et al.

However, Adam discloses a floating gate transistor with a low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al₂O₃ or transition metal oxide Ta₂O₅. Note figure 1 and column 3 line 67 of Adam. Therefore, it would have been obvious to a person having skill in the art to replace the low tunnel barrier

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intergate insulator of the floating gate transistors of Forbes et al.'s four transistor SRAM cell with the low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al_2O_3 or Ta_2O_5 such as taught by Adam in order to increase the value of the electric field between channel and gate relative to the control gate/source voltage during a write operation to thus provide a means to perform write operations at a lower voltage.

B. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over FORBES et al. (6,141,248) in view of NISHIMURA (6,069,816) and WATANABE (4,295,150).

Forbes et al. discloses a memory cell with floating gate transistors having all the limitations of claim 6 except that the low tunnel barrier intergate insulator includes a Perovskite oxide. Note figures 5B and 8A and column 5 lines 1-60 of Forbes et al.

However, Nishimura discloses a floating gate transistor with a low tunnel barrier intergate insulator that includes a ferroelectric metal oxide insulator. Note figures 3A, 3B, and 11 of Nishimura. Further, Watanabe teaches that a large number of Perovskite oxides are ferroelectric. Note column 6 line 48 of Watanabe. Therefore, it would have been obvious to a person having skill in the art to replace the low tunnel barrier intergate insulator of the floating gate transistors of Forbes et al.'s four transistor SRAM cell with the low tunnel barrier intergate insulator that includes a metal oxide insulator made from a ferroelectric material such taught by Nishimura, and specifically a Perovskite oxide such as taught by Watanabe in order to use the polariza-

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tion state "memorized" by the ferroelectric Perovskite oxide to "write" to the floating gate without the need for injecting hot electrons from the source and to "erase" the floating gate by removing the permanent polarization in the ferroelectric Perovskite oxide without the need for tunneling electrons out of the floating gate.

C. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over NISHIMURA (6,069,816) in view of ADAM (4,295,150).

Nishimura discloses a four-transistor SRAM cell with floating gate transistors having all the limitations of claim 10 except that the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al₂O₃, Ta₂O₅, TiO₂, ZrO₂, and Nb₂O₅. Note figures 3A, 3B, and 11 of Nishimura.

However, Adam discloses a floating gate transistor with a low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al₂O₃ or Ta₂O₅. Note figure 1 and column 3 line 67 of Adam. Therefore, it would have been obvious to a person having skill in the art to replace the low tunnel barrier intergate insulator of the floating gate transistors of Nishimura's four transistor SRAM cell with the low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al₂O₃ or Ta₂O₅ such as taught by Adam in order to increase the value of the electric field between channel and gate relative to the control gate/source voltage during a write operation to thus provide a means to perform write operations at a lower voltage.

D. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over RATNAKUMAR et al. (5,986,932) in view of ADAM (4,295,150).

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Ratnakumar et al. discloses a method for operating an SRAM cell having all the limitations of claim 48 except that the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al₂O₃, Ta₂O₅, TiO₂, ZrO₂, and Nb₂O₅. Note figures 4,6 and columns 9 lines 17-29 and 62-67 and column 10 lines 1-27 of Ratnakumar et al.

However, Adam discloses a floating gate transistor with a low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al₂O₃ or Ta₂O₅. Note figure 1 and column 3 line 67 of Adam. Therefore, it would have been obvious to a person having skill in the art to replace the low tunnel barrier intergate insulator of the floating gate transistors of Ratnakumar et al.'s four transistor SRAM cell with the low tunnel barrier intergate insulator that includes a metal oxide insulator made from Al₂O₃ or Ta₂O₅ such as taught by Adam in order to increase the value of the electric field between channel and gate relative to the control gate/source voltage during a write operation to thus provide a means to perform write operations at a lower voltage.

Allowable Subject Matter

11. Claims 19-27, 29-32, and 39-42 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as one or more SRAM cells, each cell comprising at least a pair of cross coupled NMOS floating gate transistors; a pair of bitlines coupled to the pair of

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cross coupled NMOS floating gate transistors at a pair of voltage nodes through a pair of access transistors; and a pair of wordlines coupled to the pair of access transistors, as recited in claims 19,24,and 29, or a method for making the same, as recited in claim 39.


12. Claims 7,8,11,12,37,38,45,46 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on M-F 8-5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9319 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
12/2002


Minh Loan Tran
Primary Examiner